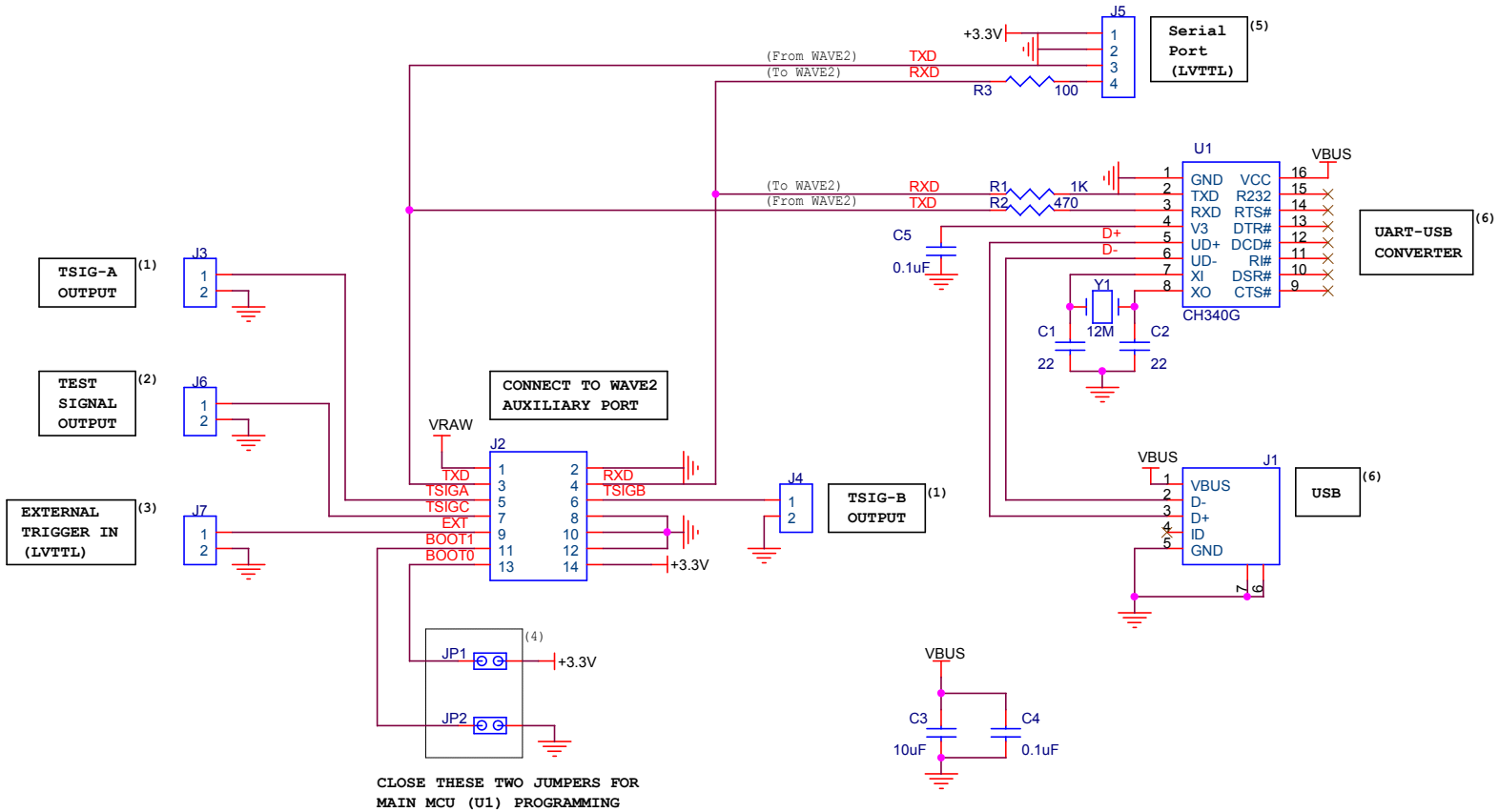


NOTES:

1. TSIG-A (J3) AND TSIG-B (J4) ARE OUTPUTS OF THE BUILT-IN FUNCTION GENERATOR.
2. TEST SIGNAL (J6) IS A 1KHZ SQUARE SIGNAL WITH AMPLITUDE OF 3.3V OR 0.14V (50% DUTY CYCLE).
3. J7 IS FOR EXTERNAL TRIGGER INPUT. THE TRIGGER LEVEL IS LVTTL LEVEL. MAXIMUM ALLOWED INPUT VOLTAGE IS 15V.
4. CLOSE JP1 AND JP2 WITH JUMPERS WHEN PROGRAMMING THE MAIN MCU (U1 INSIDE WAVE2) BY "Flash Loader Demonstrator". FOR DETAILED OPERATION STEPS PLEASE REFER TO SECTION 4 IN THE ARTICLE "How to Upgrade Firmware" UNDER DSO SHELL WEBPAGE AT WWW.JYETECH.COM.
5. J5 IS AN ALTERNATIVE CONNECTION WITH LVTTL LEVEL FOR THE SERIAL PORT. DO NOT CONNECT ANYTHING TO THIS PORT IF USB CONNECTION IS IN USE BECAUSE THE SIGNAL IN THIS PORT WILL OVERWRITE SIGNAL FROM USB PORT.
6. TO USE THE USB CONNECTION DRIVER FOR THE CHIP CH340G IS REQUIRED. WHEN USB CONNECTION IS IN USE DO NOT USE PORT J5.

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| Date: Tuesday, April 30, 2019 | Sheet 1 of 1 | |